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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,750	KOTTAPALLI, SAILESH	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Element number 510 of figure 5 and 74 and 84 of figure 7B. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method and apparatus for data speculation in an out-of-order processor utilizing test instructions and register renaming".

Claim Objections

3. Claims 7-14, and 21-28 are objected to because of the following informalities:

Claim 7 states "a advanced load instruction" in line 3 of claim. The correct statement should be "an advanced load instruction.

Claims 8-14 are objected to because of its dependency on claim 7.

Claims 11 and 14 both state "said validation circuit is an advanced load address table" in lines 1-2 whereas it is suggested to state "said validation circuit includes an advanced load address table."

Claim 21 states "a advanced load instruction" in lines 3-4 of claim. The correct statement should be "an advanced load instruction.

Claims 22-28 are objected to because of its dependency on claim 21.

Claims 25 and 28 both state "said validation circuit is an advanced load address table" in lines 1-2 whereas it is suggested to state "said validation circuit includes an advanced load address table."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Popescu et al (U.S. Patent # 5,625,837), herein referred to as Popescu et al.

As per claim 1, Popescu et al discloses a method, comprising:

issuing an advanced load instruction (This is interpreted as an actual load instruction that is valid as specified on page 6, lines 1-2 and disclosed by Popescu et al in column 8, lines 25-27) with a first instance (See column 10, lines 58-61: The first source register can be either RX or RY—depending on which results in a conflict in the example given) of a first destination register (See figure 5 and column 8, lines 25-31: Load instruction addresses are stored in the register file and is shown illustratively in figure 5);

decoding (See column 13, lines 12-15: A decoder is not explicitly disclosed but instructions are decoded and thus is indicative of a decoder) a test instruction with a second instance (See column 10, lines 58-61: Although not explicitly disclosed, there must be a second instance to result in a conflict) of said first destination register where said second instance of said first destination register is decoded as a first source register (See column 10, lines 58-61: Some instructions may result in conflicts in writing

to registers, with the first source register being either RX or RY—depending on which results in a conflict);

register renaming said first instance of said first destination register and said first source register to a first physical register (See column 9, lines 49-51: Register reallocation is used); and

validating results of said advanced load instruction using said test instruction with said first physical register (See column 11, lines 1-3: A valid bit in the result register 31 is set to indicate valid results).

As per claim 2, Popescu et al discloses wherein said test instruction is a load conditional instruction with said second instance of said first destination register (See column 8, lines 44-46: This would be one of the unsafe memory loads mentioned).

As per claim 3, Popescu et al discloses further comprising register renaming said second instance of said first destination register to a second physical register (See figure 9 and column 10, lines 45-57: The register allocation schema described and illustrated performs the same operations as claimed).

As per claim 4, Popescu et al discloses wherein said test instruction operates to move contents of said first physical register to said second physical register when said validation indicates said results are valid (See column 11, lines 3-19: Updates are done through bit changes and register updates).

As per claim 5, Popescu et al discloses wherein said test instruction is a speculation check instruction with said second instance of said first destination register (See column 16, lines 13-16: Indicative of handling cases when a speculation results in a conflict).

As per claim 6, Popescu et al discloses wherein said validating includes searching a table for an entry with said first physical register (See figure 5 and column 10, lines 58-67: A register file is searched in order to see whether results could lead to a conflict).

As per claim 7, Popescu et al discloses a processor, comprising:

a decoder (See column 13, lines 12-15: A decoder is not explicitly disclosed but instructions are decoded and thus is indicative of a decoder) to decode a test instruction with a first instance of a first destination register corresponding to a advanced load instruction with a second instance of said first destination register wherein said first instance is decoded as a first source register (See column 10, lines 58-61: Some instructions may result in conflicts in writing to registers); and

a register renaming stage to rename said second instance of said first destination register and said first source register to a first physical register (See figure 9 and column 10, lines 45-57: The register allocation schema described and illustrated performs the same operations as claimed).

As per claim 8, Popescu et al discloses wherein said test instruction is a load conditional instruction (See column 8, lines 44-46: This would be one of the unsafe memory loads mentioned).

As per claim 9, Popescu et al discloses wherein said register renaming stage to rename said first instance of said first destination register to a second physical register (See figure 9 and column 10, lines 45-57: The register allocation schema described and illustrated performs the same operations as claimed).

As per claim 10, Popescu et al discloses wherein said load conditional instruction operates to move contents of said first physical register to said second physical register when a validation circuit indicates that results of said advanced load instruction are valid (See column 11, lines 3-19: Updates are done through bit changes and register updates).

As per claim 11, Popescu et al discloses wherein said validation circuit is an advanced load address table (See figure 5 and column 10, lines 58-67: A register file used as an advanced load address table).

As per claim 12, Popescu et al discloses wherein said test instruction is a speculation check instruction (See column 16, lines 13-16: Indicative of handling cases when a speculation results in a conflict).

As per claim 13, Popescu et al discloses wherein said speculation check instruction is a no-operation when a validation circuit indicates that results of said advanced load instruction are valid (See column 6, lines 7-9: If the speculative results do not alter the state of the processor, it is the same as being a no-operation).

As per claim 14, Popescu et al discloses wherein said validation circuit is an advanced load address table (See figure 5 and column 10, lines 58-67: A register file used as an advanced load address table).

As per claim 15, Popescu et al discloses a processor, comprising:

means for issuing an advanced load instruction with a first instance of a first destination register (See figure 5 and column 8, lines 25-31: Load instruction addresses are stored in the register file and is shown illustratively in figure 5);

means for decoding (See column 13, lines 12-15: A decoder is not explicitly disclosed but instructions are decoded and thus is indicative of a decoder) a test instruction with a second instance of said first destination register where said second instance of said first destination register is decoded as a first source register (See column 10, lines 58-61: Some instructions may result in conflicts in writing to registers);

means for register renaming said first instance of said first destination register and said first source register to a first physical register (See column 9, lines 49-51: Register reallocation is used); and

means for validating results of said advanced load instruction using said test instruction with said first physical register (See column 11, lines 1-3: A valid bit is set to indicate valid results).

As per claim 16, Popescu et al discloses wherein said test instruction is a load conditional instruction with said second instance of said first destination register (See column 8, lines 44-46: This would be one of the unsafe memory loads mentioned).

As per claim 17, Popescu et al discloses further comprising register renaming said second instance of said first destination register to a second physical register (See figure 9 and column 10, lines 45-57: The register allocation schema described and illustrated performs the same operations as claimed).

As per claim 18, Popescu et al discloses wherein said test instruction operates to move contents of said first physical register to said second physical register when said validation indicates said results are valid (See column 11, lines 3-19: Updates are done through bit changes and register updates).

As per claim 19, Popescu et al discloses wherein said test instruction is a speculation check instruction with said second instance of said first destination register (See column 16, lines 13-16: Indicative of handling cases when a speculation results in a conflict).

As per claim 20, Popescu et al discloses wherein said validating includes searching a table for an entry with said first physical register (See figure 5 and column 10, lines 58-67: A register file is searched in order to see whether results could lead to a conflict).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popescu et al (U.S. Patent # 5,625,837), herein referred to as Popescu et al in view of Witt et al (U.S. Patent # 6,189,068 B1), herein referred to as Witt et al.

As per claim 21, Popescu et al teaches a system, comprising a processor including a decoder (See column 13, lines 12-15: A decoder is not explicitly disclosed

but instructions are decoded and thus is indicative of a decoder) to decode a test instruction with a first instance of a first destination register corresponding to a advanced load instruction with a second instance of said first destination register (See column 10, lines 58-61: Some instructions may result in conflicts in writing to registers) wherein said first instance is decoded as a first source register, and a register renaming stage to rename said second instance of said first destination register and said first source register to a first physical register (See column 9, lines 49-51: Register reallocation is used).

Popescu et al does not teach an interface for input-output devices, specifically an audio input-output circuit.

Witt et al does teach an interface to couple said processor to input-output devices (See column 193, lines 15-17: An interface is described), and an audio input-output circuit coupled to said interface and to said processor (See claim 13, column 196, lines 21-22).

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Popescu et al by the teachings of Witt et al to include an interface for input-output devices, specifically an audio input-output circuit, because such changes will allow the introduction of peripheral instructions and data to the processor through additions of ports and/or buses to the existing architecture; and having an interface for input-output devices can "enhance the performance of computer system" (See Witt et al on the inclusion of I/O devices, column 193, lines 19-21). Further, interfaces for input-output devices, including an interface for audio, is also

recognized as common practice for computer systems/processors at the time of the invention and is well known by people having ordinary skill in the art. Although a computer system/processor may be made to interact with itself only, one that includes the ability to communicate with peripheral devices is more commonplace and useful.

As per claim 22, Popescu et al discloses wherein said test instruction is a load conditional instruction (See column 8, lines 44-46: This would be one of the unsafe memory loads mentioned).

As per claim 23, Popescu et al discloses wherein said register renaming stage to rename said first instance of said first destination register to a second physical register (See figure 9 and column 10, lines 45-57: The register allocation schema described and illustrated performs the same operations as claimed).

As per claim 24, Popescu et al discloses wherein said load conditional instruction operates to move contents of said first physical register to said second physical register when a validation circuit indicates that results of said advanced load instruction are valid (See column 11, lines 3-19: Updates are done through bit changes and register updates).

As per claim 25, Popescu et al discloses wherein said validation circuit is an advanced load address table (See figure 5 and column 10, lines 58-67: A register file used as an advanced load address table).

As per claim 26, Popescu et al discloses wherein said test instruction is a speculation check instruction (See column 16, lines 13-16: Indicative of handling cases when a speculation results in a conflict).

As per claim 27, Popescu et al discloses wherein said speculation check instruction is a no-operation when a validation circuit indicates that results of said advanced load instruction are valid (See column 6, lines 7-9: If the speculative results do not alter the state of the processor, it is the same as being a no-operation).

As per claim 28, Popescu et al discloses wherein said validation circuit is an advanced load address table (See figure 5 and column 10, lines 58-67: A register file used as an advanced load address table).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to the method and apparatus for data speculation in an out-of-order processor utilizing test instructions and register renaming:

U.S. Patent # 5,841,998 to Isaman shows a system and method of processing instructions for a processor.

U.S. Patent # 5,854,921 to Pickett shows a stride-based data address prediction structure with validation and correction circuitry.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

3/1/06

HENRY W. H. TSAI
PRIMARY EXAMINER